REMARKS

I. General

Claims 1-13 are pending in the present application.

Claims 1-12 on file were rejected under 35 U.S.C. § 112 as failing to comply with the written description requirement.

Claims 1-12 on file were rejected under 35 U.S.C. § 103(a) as being unpatentable over Momtaz et al. (US7,263,151) in view of Moll et al. (US 7,069,488).

Claims 1, 9 and 10 have been amended. Claim 13 has been added. Support for the subject matter of new Claim 13 is found in the originally filed specification (para [12]), and in Claims 1 and 5 on file. No new matter has been added.

II. Rejection of Claims 1 and 10 under 35 U.S.C. § 112

Claims 1 and 10 were rejected in the Final Action because the phrase "comparing the sampled comparator output signal against an expected comparator output signal representing the comparator output signal without error" recited in the claims is not supported in the specification.

In response to the rejection, Applicants have amended the claims by replacing the abovementioned phrase with "an expected pattern". Support for such an amendment is found in paragraph [18] of the originally filed specification.

III. Rejection of Claims 1-12 under 35 U.S.C. § 103(a) as being unpatentable over Momtaz et al. (US7,263,151) in view of Moll et al. (US 7,069,488)

Claims 1 and 6-8

In the Final Action, Claims 1 and 6-8 have been rejected as being obvious and therefore unpatentable over Momtaz in view of Moll. Specifically, it is cited in the Final Action that

Momtaz discloses the level comparator, the sampling unit and the bit error test unit recited in Claim 1 but does not disclose "comparing the sampled comparator output signal against an expected comparator output signal representing the comparator output signal without error", now amended to be "comparing the sampled comparator output signal against an expected pattern", performed by the bit error test unit.

In response to the rejection, Applicants respectfully but strongly submit that the reference disclosures, Momtaz and Moll, do not render Applicant's invention according to Claim 1 and 6-8 obvious.

Applicants submit that "all words in a claim must be considered" (MPEP 2143.03). Applicant's Claim 1 recites "a sampling unit coupled to the level comparator and being adapted for sampling the comparator output signal" which must therefore be considered. According to the wording, the sampling unit is connected to the level comparator and is used to sample an output signal of the level comparator.

The cited col. 8, lines 50-56 of Momtaz discloses "a comparator having a first input coupled to an output of the integrator and a second input coupled to a threshold voltage, wherein the delay circuit is configured to shift the phase of the incoming data signal in a manner that is symmetrical with respect to a sampling edge of the clock signal". The comparator's output is a statistical loss of signal (SLOS) signal. (See col. 4, lines 20-22 and Figure 1 of Momtaz.) And the clock signal is applied to a flip-flop which is not connected to the comparator. (See col. 2, lines 35-52 and Figure 1 of Momtaz.) The flip flop does not sample the SLOS signal at the output of the comparator. The flip flop is merely used to latch the clock signal using delayed data. (See col. 4, lines 38-39 and Figure 2 of Momtaz.) Therefore, unlike Applicant's sampling unit that is connected to the level comparator as recited in Claim 1, Momtaz's flip-flop does not "sample the comparator output signal" as recited in Applicant's Claim 1. In other words, Momtaz does not disclose Applicant's sampling unit and its connection to the level comparator.

Moreover, Applicants submit that there is no reason for a person having ordinary skill in the art to incorporate Moll's teaching of "comparing the sampled comparator output signal against an expected pattern" into Momtaz's receiver, in light of the teaching of Momtaz.

It is cited in the Final Action that one of ordinary skill in the art would do so to "determine the presence of errors in the signal" and "therefore, accurate analysis of the signal would be performed." Applicants submit that such an accurate analysis of the signal would

render the SLOS feature of Momtaz's invention redundant. If an accurate analysis of the signal is available, there will no longer be any need for the SLOS block since information obtained from such a block can be obtained from the "accurate analysis". More importantly, Momtaz discloses the need to minimize capacitive loading on the data line and clock line introduced by the loss-of-signal circuitry. The circuitry only adds the capacitive loading of a single flip-flop to the recovered clock line, while it capacitively loads the data line by no more than the delay circuit. (See abstract, col. 2, lines19-23 and lines 30-34,.) To carry out any accurate analysis of the signal as suggested by the Examiner, additional circuitry will have to be connected to the data line and the recovered clock line of Momtaz where only the data and clock are available. Such an incorporation of additional circuitry will undoubtedly introduce further capacitive loading which may render the modified circuit unacceptable in the 10 GHz and above frequency range as disclosed in col. 3, lines 58-65 of Momtaz. Momtaz therefore teaches away from incorporating the feature of Moll into the loss-of-signal circuitry of Momtaz.

In view of the foregoing, it is submitted that Claims 1 and Claims 6-8 depending therefrom are allowable. For the same reasons, it is submitted that Claims 2-5 and 9, which variously depend from Claim 1, are also allowable. However, some of these claims are allowable for the following additional reasons.

Claim 2

Claim 2 recites "a phase shifting unit being adapted to receive and phase-shift a clock signal and to provide to the sampling unit a phase-shifted clock signal for controlling a sampling point of the sampling unit." Col. 2, lines 35-53 of Momtaz however discloses a delay circuit that is configured to shift a phase of the incoming data signal. That is, the delay circuit in Momtaz does not anticipate the phase-shifting of the clock signal as recited in Claim 2.

Claim 3

Claim 3 recites "a control unit being adapted to control the comparison level of the level comparator." On the other hand, the comparator, and thus the threshold voltage V_{TH} thereof, in Momtaz is not controlled.

Claim 4

Applicants submit that it is not clear what in Momtaz constitutes Applicants' control unit. If the clock and data recovery (CDR) block and the retimer in Momtaz are considered to anticipate Applicants' control unit, the CDR block and the retimer are not controlled at all, much less, by at least one of the bit error test unit and an interface unit adapted to be coupled to a unit external with respect to the integrated circuit as recited in Claim 4.

Claim 5 and new Claim13

Claim 5 recites "an input unit adapted to receive an input signal from external with respect of the integrated circuit" and the input unit includes the level comparator and the sampling unit. The level comparator receives the input signal as the comparator input signal. The comparator in Momtaz however receives a signal output from an integrator. The output of the integrator is not an input signal external to Applicants' integrated circuit.

The integrated circuit may also include "a processing unit adapted to receive and process the sampled comparator output signal" and "an output unit adapted to receive a data signal from the processing unit, to derive therefrom an output signal, and to provide the output signal to external with respect of the integrated circuit". Momtaz does not disclose any processing unit or output unit. For the same reason, Claim 13 which is the combination of the subject matter of Claim 1 and Claim 5 is also allowable.

Claim 9

Claim 9 recites "the sampling unit comprises a deserializer adapted for deserializing the comparator output signal". This deserializer deserializes the high speed comparator output signal COS to a lower speed signal. (See para [28].) Again, Momtaz does not disclose such a deserializer.

Claims 10 - 12

The amended Claim 10 now recites a method in an integrated circuit. The method includes "comparing a level of a comparator input signal with a comparison level and correspondingly providing a comparator output signal, sampling the comparator output signal, and determining from the sampled comparator output signal an indication of a bit error in a sequence of the sampled comparator output signal by comparing the sampled comparator

output signal against an expected pattern. It is cited in the Final Action that Momtaz discloses all steps of Claim 10 except the comparing of the sampled comparator output signal against an expected pattern. As explained above under Claim 1, the cited col. 8, lines 50-56 of Momtaz discloses "a comparator having a first input coupled to an output of the integrator and a second input coupled to a threshold voltage, wherein the delay circuit is configured to shift the phase of the incoming data signal in a manner that is symmetrical with respect to a sampling edge of the clock signal". The comparator's output is a statistical loss of signal (SLOS) signal. (See col. 4, lines 20-22 and Figure 1 of Momtaz.) And the clock signal is applied to a flip-flop, and this flip flop is not connected to the comparator. (See col. 2, lines 35-52 and Figure 1 of Momtaz.) The flip flop does not sample the SLOS signal at the output of the comparator. The flip flop is merely used to latch the clock signal using delayed data. (See col. 4, lines 38-39 and Figure 2 of Momtaz.) Therefore, unlike Applicant's sampling unit, Momtaz's flip-flop does not "sample the comparator output signal" as recited in Applicant's Claim 1.

For the same reasons given under Claim 1, Applicants submit that there is no reason for a person having ordinary skill in the art to incorporate Moll's teaching of "comparing the sampled comparator output signal against an expected pattern" into Momtaz's receiver, in light of the teaching of Momtaz.

In view of the foregoing, it is submitted that Claims 1 and 12 are allowable.

For the same reasons, it is submitted that Claim 11, which depends from Claim 10, is also allowable. However, Claim 11 is allowable for the additional reason given under Claim 3.

CONCLUSION

In view of the discussions set forth herein, it is respectfully submitted that the grounds for the Examiner's objections and rejections have been overcome. Accordingly, it is respectfully submitted that Claims 1-13 should be found to be in condition for allowance.

Respectfully submitted,

/Marc Bobys/

Marc Bobys
Reg. No. 45,267
MB/SWN

Tel.: +65 6215 8672

Dated: July 14, 2008

AGILENT TECHNOLOGIES, INC.
Legal Department, M/S DL 429
Intellectual Property Administration
P.O. Box 7599
Loveland, Colorado 80537-0599